## REMARKS

### Amendments

***Amendments to the Claims***

Applicant has amended claims 2, 11, 16 and 23. No new matter has been added because support for the amendments can be found, *intra alia*, at page 12. lines 10-12 of Applicant's specification as originally filed.

### Rejections

***Rejections under 35 U.S.C. § 103(a)***

**Claims 2-8, 11-14, 16-21, and 23-26**

Claims 2-9, 11-14, 16-21, and 23-26 stand rejected under 35 U.S.C. § 103(a) as being obvious over Stortz U.S. Patent No. 5,900,885 in view of by Priem et al., European Patent Application 0 525 986 (both previously cited). Applicant respectfully submits that this combination is improperly motivated and does not teach each and every element of the invention as claimed in claims 2-9, 11-14, 16-21, and 23-26.

Stortz discloses using system memory and/or video memory to provide a composite frame. The composite video frame comprises interleaved portions read from dedicated and incremental video buffers. The controller interleaves the contents of the dedicated and incremental video buffers to produce a single interlaced video frame. Because the controller interleaves the data, each buffer contains only data for part of the video frame. The motivation of Stortz's architecture is to augment dedicated video memory without requiring additional memory or a new video memory controller card as well as not wasting video memory (Stortz, Col. 1, lines 24-27; Col. 2, lines 11-14). Thus, the intended purpose of Stortz's controller is to provide a composite frame by reading from both buffers to create a single video frame. Furthermore, Stortz discloses the video controller comprises a dynamic random access memory (DRAM) buffer.

Priem discloses three different double buffered display systems each comprising a central processing unit (CPU) with two frame buffers. The first system comprises a single memory controller and two video random access memory (VRAM) buffers. In this

display system, the central processing unit writes a frame of data to one of the frame buffers and the digital-to-analog converter (DAC) reads another frame of data from the other frame buffer. A multiplexor controls which of the two frame buffers supplies the data to the DAC.

Priem's other two display systems replace one of the VRAM buffers with a less expensive DRAM buffer. The second display system utilizes one memory controller for both buffers. In this system, the system writes a frame of data to the DRAM buffer and then copies this frames over to the VRAM buffer. The display is fed the frame stored in the VRAM buffer. However, by using one controller, this second system suffers from "frame tearing," because the bandwidth of the DRAM buffer cannot sustain the refresh rate of the VRAM buffer (Priem, Col. 7, lines 38-53). To overcome this "frame tearing" problem, Priem discloses a third display system with two controllers, one for each buffer. However, Priem does not disclose in any of the three display systems having one or both frame buffers as part of the general main system memory.

Thus, Priem discloses that a display system with a single memory controller and a DRAM buffer that suffers from frame tearing. Display systems that use two memory controllers or use a VRAM buffer in place of the DRAM buffer do not suffer from frame tearing.

Applicant respectfully submits that the combination of Stortz and Priem is improperly motivated. "If the proposed modification or combination of the prior art would change the principle of operation of the prior invention being modified, then the teachings of the references are not sufficient to render the claim *prima facie* obvious" (MPEP § 2143.01(VI)). The Examiner admits that Stortz does not disclose writing a full frame of color data into the frame preparation memory. The Examiner proposes to overcome this deficiency of Stortz by substituting Stortz's system memory video buffer with Priem's VRAM buffer from the Priem's first display system that is multiplexed to the display (Office Action, page 4). However, a combination of this type changes the principle of Stortz's operation. Stortz reads from two buffers to directly feed the display whereas Priem reads from only one buffer. Combining Stortz with Priem's full frame buffer renders Stortz's second buffer unnecessary because Priem's full frame buffer holds an entire frame of data. As a result, this combination reads directly for the full frame

buffer and not the two buffer originally taught by Stortz. Thus, because this combination reads from only one buffer, the combination modifies Stortz's principle of operation by reading from only one buffer instead of two. Therefore, the proposed combination changes the principle operation of Stortz and the combination teachings are not sufficient to render claims 2-9, 11-14, 16-21, and 23-26 *prima facie* obvious.

Furthermore, "if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification" (MPEP § 2143.01(V)). The intended purpose of Stortz's controller is to provide a composite frame by reading from both buffers so as to augment the dedicated video memory. However, the proposed combination changes this intended purposed because, as per above, the combination only reads from one buffer and not two buffers as intended by Stortz. Therefore, the proposed combination renders Stortz unsatisfactory for Stortz's intended purpose and there is no suggestion or motivation to make the proposed modification.

In addition, the combination of Stortz and Priem is improperly motivated because Priem teaches away from using single controller with a DRAM buffer. "It is improper to combine references where the references teach away form the combination" (MPEP § 2145(X)(D)(3)). In particular, the Examiner proposes replacing Stortz's system memory buffers with one of Priem's buffers because the Examiner admits that Stortz does not disclose writing a full frame of color data into the frame preparation memory. Because Applicant's frame preparation memory is mapped onto system memory, Priem's VRAM buffers cannot be used as a substitute for Stortz's buffer as one of skill in the art would know that VRAM is not used for system memory. Thus, Priem's DRAM buffer is used in the combination. Furthermore, this combination of Stortz and Priem would utilize Stortz's one memory controller to read and write to Priem's DRAM buffer.

However, Priem explicitly teaches that a single memory controller system reading and writing to a DRAM buffer cannot keep up with a frame rate required by the display. Thus, Priem teaches away from using a single controller system, such as Stortz. Because Priem discloses that single controller systems cannot keep up with a frame rate required by a display, there is no motivation to combine Priem with Stortz.

Therefore, there is no motivation to combine Stortz and Priem. Suggesting that

these references are combinable relies of impermissible hindsight based on the applicants' disclosure.

Nonetheless, assuming for the sake of argument that if the combination is properly motivated, the combination fails to teach or suggest each and every element as claimed. With regards to claims 2, 11, 16, and 23, Applicant claims a full frame of color data that is written into the frame-preparation memory at frame rate, where the frame-preparation memory has a bandwidth that supports the refresh rate. The Examiner admits that Stortz does not disclose writing a full frame of color data into the frame preparation memory. Thus, Stortz cannot teach or suggest the claimed element.

As per above, Priem's VRAM buffer cannot be properly interpreted as disclosing Applicant's frame preparation memory mapped into system memory. As for Priem's DRAM buffer, Priem does not disclose that this DRAM buffer is mapped into main memory. Priem discloses that the DRAM buffer is merely a substitute for a second VRAM buffer that is part of a graphics subsystem and, thus, is not part of main memory. Moreover, it is not necessary that a DRAM buffer be considered as part of main memory. For example, Stortz discloses a DRAM buffer that is part of the video controller (See Stortz, Fig. 1, #20 and #22). Therefore, neither Priem's DRAM nor his VRAM buffer can be properly interpreted as disclosing Applicant's frame-preparation memory as claimed.

Even assuming, *arguendo*, that Priem's DRAM buffer can be equated to Applicant's frame preparation memory, Priem does not teach or suggest that Priem's DRAM buffer has the memory bandwidth to support the refresh rate. Priem discloses that using a single memory controller system with the DRAM buffer suffers from frame tearing.[1] This frame tearing is due to the DRAM buffer having a single port and the system cannot transfer data fast enough from the DRAM buffer to the VRAM buffer to support the display refresh rate. Thus, Priem's DRAM buffer does not have the memory bandwidth to support the refresh rate. Therefore, Priem cannot be properly interpreted as teaching or suggesting "a full frame of color data that is written into the frame-

---

[1] The Examiner asserts that "the fact that Priem discloses two memory controllers does not affect that reasoning of operating upon full frames of data" (Office Action, p. 10). Applicant respectfully disagrees. If the Examiner is relying on two memory controllers for the combination, then the combination fails to have a sole memory controller as claimed in independent claims 2, 11, 16, and 23.

preparation memory at frame rate, the frame-preparation memory having a bandwidth that supports the refresh rate" as claimed.

Thus, the combination cannot be properly interpreted as disclosing claims 2, 11, 16, and 23 and claims 3-8, 12-14, 17-21, and 24-26 that depend on them. Therefore, the combination cannot render obvious Applicant's invention as claimed in claims 2-9, 11-14, 16-21, and 23-26, and Applicant respectfully requests the withdrawal of the rejection of the claims under 35 U.S.C. § 103(a) over the combination.

## SUMMARY

Claims 2-9, 11-14, 16-21 and 23-26 are currently pending. In view of the foregoing remarks, Applicant respectfully submits that the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Eric Replogle at (408) 720-8300 x7514.

**Deposit Account Authorization**

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR
& ZAFMAN LLP

Dated: July 1, 2008

Eric S. Replogle
Registration No. 52,161

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300